Appendix 9
Postprocessors nrl and nzd

Programs **nrl** (no repeating lines) and **nzd** (no zero delay) are used to **postprocess the file with results of Alecsis <u>digital</u> simulation**, i.e file with extension '.ar'. You can call them in the following way:

```
nrl file_name.ar
nzd file_name.ar
```

It is necessary to type the extension '.ar'.

Input of these programs is the output file of the program Alecsis. The output is file with the same name - previous content is erased. If the content is to be saved, it should be copied before, under a different name. In case you forget to do this, you can always replay the simulation and regenerate the output file.

In digital simulation, results are printed whenever there is an event on traced signals. Some of these events can be **neutral events**, having no effect on the output drivers. They are printed out by Alecsis, but apart for giving information about neutral events, these lines are useless and reduce readability of the output file. Postprocessor **nrl** removes all repeating lines (only one copy of a line is left). **Line is considered as repeating, if all traced signals have the same value as in the previous line, and the value of the simulation time is the same as in the previous line.**

Processor **nzd** removes all lines with the same value of simulation time, except the last one. When a digital circuit is simulated using **zero delay**, there can be such lines in the output file. Such events cannot be viewed on the graphics anyway, as they are drawn for the same time instant.

The effects of these processors are shown on an example. Simulation output file `test.ar` has the following content:

```
adder_15_test

OutputVariables:
TIME   0:x[0] 0:x[1] 0:x[2] 0:s 0:c_out 0:ncout

OutputValues:

0.0000e+00  0  0  0  *  *  *
0.0000e+00  0  0  0  *  *  1
0.0000e+00  0  0  0  *  0  1
0.0000e+00  0  0  0  *  0  1
0.0000e+00  0  0  0  0  0  1
1.0000e+00  0  0  0  0  0  1
2.1000e+00  0  0  1  0  0  1
2.1000e+00  0  0  1  0  0  1
2.1000e+00  0  0  1  1  0  1
3.0000e+00  0  1  0  1  0  1
3.0000e+00  0  1  0  1  0  1
3.0000e+00  0  1  0  0  0  1
3.0000e+00  0  1  0  0  0  1
3.0000e+00  0  1  0  0  0  1
3.0000e+00  0  1  0  1  0  1
4.0000e+00  0  1  1  1  0  1
4.0000e+00  0  1  1  1  0  1
4.0000e+00  0  1  1  0  0  0
4.0000e+00  0  1  1  0  1  0
5.0000e+00  1  0  0  0  1  0
5.0000e+00  1  0  0  0  1  0
5.0000e+00  1  0  0  1  1  1
5.0000e+00  1  0  0  1  0  1
```

After execution of the command:

nrl test.ar

file `test.ar` has the following content:

```
adder_15_test

OutputVariables:

TIME   0:x[0] 0:x[1] 0:x[2] 0:s 0:c_out 0:ncout

OutputValues:

0.0000e+00  0  0  0  *  *  *
0.0000e+00  0  0  0  *  *  1
0.0000e+00  0  0  0  *  0  1
```

```
0.0000e+00   0   0   0   0   0   1
1.0000e+00   0   0   0   0   0   1
2.1000e+00   0   0   1   0   0   1
2.1000e+00   0   0   1   1   0   1
3.0000e+00   0   1   0   1   0   1
3.0000e+00   0   1   0   0   0   1
3.0000e+00   0   1   0   1   0   1
4.0000e+00   0   1   1   1   0   1
4.0000e+00   0   1   1   0   0   0
4.0000e+00   0   1   1   0   1   0
5.0000e+00   1   0   0   0   1   0
5.0000e+00   1   0   0   1   1   1
5.0000e+00   1   0   0   1   0   1
```

After execution of the command:

```
nzd test.ar
```

file `test.ar` has the following content:

```
adder_15_test

OutputVariables:

TIME   0:x[0] 0:x[1] 0:x[2] 0:s 0:c_out 0:ncout

OutputValues:

0.0000e+00   0   0   0   0   0   1
1.0000e+00   0   0   0   0   0   1
2.1000e+00   0   0   1   1   0   1
3.0000e+00   0   1   0   1   0   1
4.0000e+00   0   1   1   0   1   0
5.0000e+00   1   0   0   1   0   1
```